IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	DANIEL B. REENTS PATRICK MAUPIN	Group Art Unit:	2133
		Examiner:	CHASE, SHELLY A.
Serial No.:	09/375,120	Conf. No.:	4618
Filed:	AUGUST 16, 1999	Atty. Dkt.:	2000.012600/TT2670
For:	METHOD AND APPARATUS FOR ADAPTIVE FRAME TRACKING	CUSTOMER NO.	23720

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	7-5-05

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Nancy Nolan
Signature

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On May 2, 2005, Appellants filed a Notice of Appeal in response to a Final Office Action dated January 31, 2005, issued in connection with the above-identified application. In support of the appeal, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on May 5, 2005, the two-month date for filing this Appeal Brief is July 5, 2005. Since this Appeal Brief is being filed on July 5, 2005, this paper is believed to be timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500.00) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT2670. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT2670.[1]

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-41 remain pending in this application.

[1] In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.012600.

The Examiner rejected claims 1-7 and 37-41 under 35 U.S.C. § 103(a) as being unpatentable by 5,958,027 (***Gulick***), in view of U.S. Patent No. 6,021,129 (***Martin***). The Examiner objected to claims 8-36.

The claims currently under consideration, *i.e.*, claims 1-41, are listed in the Claims Appendix submitted herewith.

IV. STATUS OF AMENDMENTS

After the Final Rejection, amendments to claims 37 and 41 were made but were not entered by the Examiner. Claims 37 and 41 are presented in the form prior to the amendments that were proposed in response to the Final Rejection. After the Final Rejections, no other amendments were made to any other claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides for an apparatus for performing adaptive frame tracking, The apparatus includes an adaptive frame tracking unit that is capable of receiving and sending data packets. The adaptive frame tracking unit is capable of automatically adjusting a data rate of the data packet in response to a determination that at least one data frame error exists. The adaptive frame tracking unit is also capable of correcting for the data frame error.

The use of Universal Serial Bus (USB) systems in the field of computer technology has improved computer usage and computer communications. Implementing USB-related solutions for computer technology can result in improvements in the quality and efficiency of computer system usage. The present invention provides for a method and apparatus for efficiently

recovering from data packet framing errors, particularly start of frame errors. The present invention also provides for a computer software solution for determining a frame number of the data packet being transmitted on a USB system. Furthermore, the present invention provides for an automated method of adjusting a data rate of isochronous data transfers. The methods described by the present invention may be implemented through software, hardware, or firmware technologies. The methods described by the present invention may also be implemented by any combination of software, hardware, and firmware technologies. *See* Detailed Description Section of Specification, page 6, line 24 – page , lines 1-10.

Generally, packets of data are transmitted to and from a computer system and computer peripherals. The packets of data being transmitted generally contain start of frame sections, which contains information regarding the data packets being transmitted. In one embodiment, a USB system device, such as a USB host (not shown), transmits a set of generic data patterns along with specific, unique data. In one embodiment, the USB host is a computer system. The set of generic data patterns include uniform data patterns that aid computer systems in identifying a data packet, synchronizing the reception of data, and identifying the end of a particular data pattern. In one embodiment, a packet of data that is transmitted via a USB communication system includes a packet identification data pattern within the packet of data. In one embodiment, the packet identification data pattern is a start of frame (SOF) data pattern. Generally, a start of frame is sent by a USB host at a rate of once per frame of USB data. *See* Detailed Description Section of Specification, page 7, lines 12-23.

Turning now to Figure 1, one embodiment of the apparatus, an adaptive frame tracking unit 110, of the present invention is illustrated. In one embodiment, digital logic circuits that are encompassed in the adaptive frame tracking unit 110 to operate in sync with the USB bit time clock on a line 120. A system reset signal on a line 130 is capable of resetting the logic functions of the digital logic circuits that are encompassed in the adaptive frame tracking unit 110. The adaptive frame tracking unit 110 receives a USB start of frame signal on a line 140 and performs digital functions to produce several digital signals for performing adaptive frame tracking. The adaptive frame tracking unit 110 also receives a frame number signal on a line 145. The digital signals generated by the adaptive frame tracking unit 110 includes the frame position updated signal on a line 150, a latched frame count signal on line 160, a frame position monitor sample clock on a line 165, an isochronous packet size signal on a line 170, a latched frame number signal on a line 180, and a time stamp match signal 190. In one embodiment, the steps comprising adaptive frame tracking is illustrated in Figure 2. *See* Detailed Description Section of Specification, page 8, lines 1-14.

In one embodiment, the method and apparatus of the present invention monitors a USB start of frame data pattern. The adaptive frame tracking unit 110 is employed to support multiple data synchronization functions required by the USB system while it is transmitting or receiving data via the USB. In one embodiment, the start of frame packet sent by a host USB includes a sync data field, a packet identification data field, a frame number field, a CRC5 bit, and an end of packet (EOP) data field. In one embodiment, the frame number data field comprises of a twelve-bit data field. In one embodiment, the function of monitoring the start of frame data

packet is important in supporting isochronous data transfers. *See* Detailed Description Section of Specification, page 8, lines 16-23.

Isochronous data generally refers to time-dependant data. In other words, isochronous data transfer refers to processes where data is transmitted and received within certain time constraints. In one example, for multimedia data communications, an isochronous transport mechanism is generally required since data must be delivered as fast as it is displayed such that audio and video signals are synchronized. In contrast, asynchronous data transmission generally refers to processes in which random intervals can exist between transmission of packets of data. In further contrast with isochronous data transmission, synchronous data transmission can generally only be received or sent during specific intervals. Isochronous data transmission generally does not require a rigid protocol such as the one that is generally required for transmission of synchronous data. However, isochronous data transmission generally requires a more rigid protocol than the one required by the transmission of asynchronous data. *See* Detailed Description Section of Specification, page 9, lines 1-12.

Turning now to Figure 2, a block diagram depiction of the primary tasks performed by the method and apparatus of the present invention, is illustrated. One of the primary functions of the adaptive frame tracking unit 110 is to monitor the USB start of frame data pattern, as described in block 210 of Figure 2. The adaptive frame tracking unit 110 supports a transmit data buffering function, as described in block 220 of Figure 2. Buffering the transmitted data allows the adaptive frame tracking unit 110 to control the USB data flow rate. The adaptive frame tracking unit 110 also determines whether at least one isochronous data packet was

missed, as described in block 230 of Figure 2. The adaptive frame tracking unit 110 also establishes a data rate for the start of frame, as described in block 240 of Figure 2. The adaptive frame tracking unit 110 is capable of providing an automated data rate control for data transmission on a USB system, as described in block 250 of Figure 2. *See* Detailed Description Section of Specification, page 8, lines 14 – 24.

The adaptive frame tracking unit 110 is capable of monitoring an USB system for a start of frame data packet and generating a start of frame data packet if one is not received. The start of frame data packet may be missing during data transmission for various reasons including the reasons that the USB host may not send a start of frame data packet or data on the USB has been corrupted. The creation of a start of frame data packet is generally known as start of frame synthesis. Turning now to Figure 3, more detailed block diagram depiction of the adaptive frame tracking unit 110, is illustrated. In one embodiment, the adaptive frame tracking unit 110 includes a start of frame synthesizer circuit 310, a frame position monitor circuit 320, a frame number monitor circuit 330, and an auto data rate control circuit 340. *See* Detailed Description Section of Specification, page 6, line 1 – 9.

The start of frame synthesizer circuit 310 generates a frame count signal on a line 350, which is sent to the frame position monitor circuit 320. The frame position monitor circuit 320 generates a frame position updated signal on the line 150, which is used to latch the frame count signal and create the latched frame count signal on the line 160. The frame position monitor 320 also generates a frame position monitor sample clock on a line 165. The start of frame synthesizer circuit 310 also generates a synthesized start of frame signal on a line 360, which are

sent to the frame number monitor circuit 330 and the auto data rate control circuit 340. The auto data rate control circuit 340 generates an isochronous packet size signal on the line 170. The start of frame synthesizer circuit 310 also generates a missed start of frame signal on a line 370, which is sent to the frame number monitor circuit 330. The frame number monitor circuit 330 generates the latched frame number signal on the line 180, and the time stamp match signal on the line 190. The signals generated by the adaptive frame tracking unit 110 can be used in combination with a USB host to perform start of frame synthesis, start of frame monitoring, automatic data rate control, and other adaptive frame tracking tasks. *See* Detailed Description Section of Specification, page 10, lines 11–25.

Turning now to Figure 4, one embodiment of a more detailed depiction of the start of frame synthesizer circuit 310, is illustrated. The start of frame synthesizer circuit 310 employs an adaptive frame tracking method to monitor data streams on the USB system to check for start of frame data patterns. The start of frame synthesizer circuit 310 is capable of detecting a missing start of frame data pattern. In one embodiment, the start of frame synthesizer circuit 310 then synthesizes a new start of frame data pattern and adds it to the data stream. The start of frame synthesis, in one embodiment, causes the start of frame interval length to be approximately the same as the start of frame interval length of the previous successfully received start of frame data pattern. *See* Detailed Description Section of Specification, page 11, lines 1-10.

The start of frame synthesizer circuit 310 employs two counters, the frame counter 410 and the error counter 420, to track the number of bits in a particular frame of data. In one embodiment, the frame counter is incremented by the USB bit time clock on the line 120. The

frame counter 410 is reset each time a start of frame is detected or each time a start of frame is synthesized. The output of the frame counter 410 is used to generate the frame count signal on a 350, which is sent to the frame position monitor circuit 320. *See* Detailed Description Section of Specification, page 11, lines 11 – 17.

The error counter 420 is incremented or decremented based upon the number of bits in the data frame. The incrementing and the decrementing of the error counter 420 allow the synthesized start of frame length to be adaptable to the actual start of frame length. The outputs of the frame counter 410 and the error counter 420 are used to generate the synthesized start of frame signal on a line 360, which is sent to the auto data rate control circuit 340 and the frame number monitor circuit 330. In one embodiment, the synthesized start of frame signal on the line 360 is generated at approximately the same equivalent period of time as the previous start of frame data packet. *See* Detailed Description Section of Specification, page 11, line 19 – page 12, lines 1-2.

The synthesized start of frame signal on the line 360 is generated earlier than the equivalent period of time as the previous start of frame data packet when the start of frame data packet is received before the expected time. Furthermore, the frame count signal on the line 350 is decremented when the start of frame data packet is received before the expected time period. The synthesized start of frame signal on the line 360 is generated at approximately the period of time as the previous start of frame data packet when the start of frame data packet is received later than the expected time period. The frame count signal on the line 350 is incremented when the start of frame data packet is received later than the expected time. The frame count signal on

the line 350 is not incremented or decremented when the start of frame data packet is received at the expected time period. In one embodiment, an additional missed start of frame signal on the line 370 is generated when the start of frame data packet is not received within a predetermined period of time period after the start of frame data packet was expected. *See* Detailed Description Section of Specification, page 12, lines 4– 16.

Generally, synchronized isochronous data endpoints synchronize their data to approximately match the data rate of the USB host. In one embodiment, an isochronous data endpoint (endpoint) is a computer peripheral device. The adaptive frame tracking unit 110 is capable of monitoring USB start of frame data packet rate and modify the start of frame data packet rate to synchronize to the data rate of the USB host. In one embodiment, an external output that reflects the internally synthesized start of frame signal, is provided. The signal allows an external computer peripheral device, such as a digital signal processor (DSP), to monitor the data rate of the USB start of frame data packet. When the data rate of the USB host start of frame data changes, the data rate of the isochronous endpoint is changed to track or adapt to the data rate of the USB host start of frame data. The adaptation of the data rate of the isochronous to the data rate of the USB host start of frame data is generally called adaptive synchronization. *See* Detailed Description Section of Specification, page 12, line 18 - page 13, lines 1-4.

In another embodiment, the adaptive frame tracking unit 110 is capable of synchronizing its data rate to a USB bit time clock on the line 120. This synchronization is performed by the adaptive frame tracking unit 110 by monitoring the data rate of USB data frames and requesting the USB host to change its data rate accordingly. In other words, the adaptive frame tracking

unit 110 requests the USB host to change the number of USB data clocks in a single USB frame of data, thereby changing the USB data frame interval. The adaptation of the USB data frame interval is generally known as start of frame mastership. The frame position monitor circuit 320 is provided to allow the adaptive frame tracking unit 110 to perform the start of frame mastership. *See* Detailed Description Section of Specification, page 13, lines 6-14.

Turning now to Figure 5, a more detailed embodiment of the frame position monitor circuit 320 is illustrated. In one embodiment, the frame position monitor circuit 320 monitors two different input clocks, and selects one clock to be a sample clock signal on a line 510. The frame monitor position circuit 320 detects the positive edge of the sample clock signal on a line 510, synchronizes the sample clock signal, and generates a single clock-wide frame position monitor sample clock on the line 165. Utilizing a dividing counter 540, the frame position monitor circuit 320 is capable of dividing the frame position monitor sample clock on the line 165 by 1, 2, 4, 8, 16, 32, or 64 times. The dividing factor used to divide the frame monitor sample clock on the line 165 is selected by the sample clock rate select signal on a line 550. The frame position monitor circuit generates a frame position updated signal on a line 150 and utilizes this signal to latch the frame count signal on the line 350 to generate the latched frame count signal on the line 160. The frame count signal on the line 350 is latched into the frame count register 360. The latched frame count signal on the line 160 is latched on the positive edge of the divided frame position sample clock. *See* Detailed Description Section of Specification, page 13, line 16 – page 14, lines 1-4.

The latched frame count signal on the line 160 represents the data rate from a source, such as a computer peripheral plugged into a USB port of a computer system. The latched frame count signal can be read by the central process unit (CPU) (not shown) of a USB host. Software in a computer peripheral device can determine how its data rate is changing relative to a USB data clock by examining the latched frame count signal on the line 160 at various programmable time periods of the sample clock on the line 510 and request to the USB host to modify the USB data rate. *See* Detailed Description Section of Specification, page 14, line5-12.

Turning now to Figure 6, a more detailed embodiment of the auto data rate control circuit 340, is illustrated. Utilizing the auto data rate control circuit 340, the adaptive frame tracking unit 110 is capable of automatically controlling the data rate of an isochronous data endpoint by using the data sample rate of the source, such as a computer peripheral, and the USB data frame rate. This is one form of adaptive data synchronization called auto rate control. The auto rate controller circuit 340 uses the frame position monitor sample clock on the line 165 to increment an auto rate counter 610. The auto rate counter 610 is incremented and cleared by the auto rate controller 620. The auto rate counter 610 is clocked by the USB bit time clock signal on the line 120. When the auto rate control circuit 340 receives the synthesized start of frame signal on the line 360, the count value in the auto rate counter 610 is latched into an auto rate register 630. The count value from the auto rate counter 610 is latched into the auto rate register 630 by a count value latch signal on a line 635, which is generated by the auto rate controller 620. The auto rate counter 610 is then cleared and re-enabled by the auto rate controller 620. The latched count value from the auto rate counter 610 is then multiplied by 1, 2, or 4 by a left-shifter multiplier 640 and presented to the data endpoints as the isochronous packet size signal on the

line 170. The multiplication factor used by the left-shifter multiplier 640 is controlled by the left shifter select signal on a line 650. *See* Detailed Description Section of Specification, page 14, line 14 – page 15, lines 1-6.

The isochronous packet size signal on the line 170 is used to automatically select the number of bytes that the isochronous endpoint will return to the USB host during the next IN transaction from the endpoint. The left shifter multiplier 640 is provided to support data sources that have more than one byte of data per sample. In one embodiment, the mechanism described in Figure 3 is implemented under an assumption that when the synthesized start of frame signal on a line 360 is generated, data that is to be sent to the USB host from a particular IN endpoint resides in a memory section (not shown) of a USB system. A plurality of data management systems that are known to those skilled in the art, may be employed to manage data movement processes between the memory section and a data endpoint. *See* Detailed Description Section of Specification, page 15, lines 8-16.

Turning now to Figure 7, a more detailed depiction of the frame number monitor circuit 330, is illustrated. A start of frame data packet generally contains a USB frame number value, which is placed on the USB frame number signal on the line 145. The USB frame number signal on the line 145 is passed to a peripheral device, from the USB host, in each start of frame data packet that is successfully received by the peripheral device. The USB frame number value contained in the start of frame data packet is latched each time the synthesized start of frame signal on the line 360 is asserted. The frame number monitor circuit 330 latches the USB frame number signal using a frame number monitor counter 710 and generates the latched USB frame

number signal on a line 720. The USB frame number signal may be then read to determine the present frame number value. *See* Detailed Description Section of Specification, page 15, lines 18 – page 16, lines 1-2.

In one embodiment, the USB frame number signal may not be latched if a start of frame data packet is not received by the computer peripheral device in a particular frame of data. When a start of frame data packet is missing from a frame of data, the start of frame synthesizer circuit 310 generates the missed start of frame signal on the line 370, which is sent to the frame number monitor circuit 330. When the missed start of frame signal on the line 370 is asserted, the frame number monitor counter 710 increments the previously latched USB Frame number signal on the line 710, by one. *See* Detailed Description Section of Specification, page 16, lines 4-10.

The frame number monitor circuit 330 includes a time stamp match register 730 that can be loaded, through a time stamp match signal on a line 740, by the USB system software. The time stamp match register 730 is utilized to generate a time stamp match signal on a line 750 when the latched frame number signal on the line 720 is equal to or greater than the time stamp match value signal on the line 740. In one embodiment, the time stamp match value is loaded into the time stamp register through the time stamp match signal on the line 750. In one embodiment, the time stamp match signal on the line 750 will be generated until the time stamp match register 730 is written again. In one embodiment, generating the latched frame number signal on the line 720 and the time stamp match signal on the line 750, provides the USB system software information regarding the frame number of the corrupted or missing start of frame data

packet. The principle taught by the present invention may be utilized for other type of data communication systems. *See* Detailed Description Section of Specification, page 16, lines 12 – 23.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-7 and 37-41 are unpatentable under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,958,027 (***Gulick***), in view of U.S. Patent No. 6,021,129 (***Martin***).

VII. ARGUMENT

The present invention is directed to providing an apparatus and method of automatically adjusting a data rate of a data packet by determining if there exists a data frame error. The present invention provides for correcting the data frame error in response to a determination that the data frame error exists. The present invention provides for an adaptive frame tracking unit 110 to support multiple data synchronization functions required by an USB system while it is transmitting or receiving data via the USB. *See*, Specification, page 8, lines 16-23. The start of frame packet sent by a host USB may include a sync data field, a packet identification data field, a frame number field, a CRC5 bit, and an end of packet (EOP) data field. *Id.* The adaptive frame tracking unit 110 may determine whether at least one isochronous data packet was missed. *See*, Figure 2 and Specification, page 9, lines 14-24. The adaptive frame tracking unit 110 also establishes a data rate for the start of frame. *Id.* The adaptive frame tracking unit 110 is capable of providing an automated data rate control for data transmission on a USB system. *Id.*

The Examiner relies heavily upon ***Gulick*** to reject the pending claims in the instant patent application. Further, the Examiner also relies upon ***Martin*** to make up for the deficit of ***Gulick***. The Examiner had asserted the position that ***Gulick*** does not disclose automatically adjusting the clock rate of a transmission rate. ***Martin*** does not disclose frame tracking and adjusting a data rate based upon a data frame error. Therefore, Appellants respectfully assert that since ***Gulick*** does not disclose adjusting a clock rate based upon a transmission rate, and ***Martin*** does not disclose frame tracking and adjusting a data rate based upon a data frame error, the combination of ***Gulick*** and ***Martin*** could not possibly disclose or make obvious automatically adjusting the data rate based upon a data frame error, as called for by claims of the present invention.

Martin clearly does not disclose automatically adjusting a data rate based upon a data frame error. Further, nowhere does ***Gulick*** disclose adjusting a data rate based upon a data frame error. The mere disclosure in ***Gulick*** disclosing that a mechanism is provided to adjust the clock rate of a data producer to match the data clock rate of a USB host does not read upon elements of the claims of the present invention. *See* column 7, lines 35-37. ***Gulick*** merely discloses that the clock rate of the data producer is adjusted and it is not practical to adjust the data base of a USB host. *See* column 7, lines 37-39. This disclosure does not make obvious automatically adjusting a data rate of a data packet based upon a data frame error. Various elements of the claims of the present invention are not disclosed, taught, or suggested by ***Martin***, ***Gulick*** or their combination, contrary to the Examiner's contentions in the Final Office Action dated January 31, 2005. Therefore, the Examiner erred in rejecting claims 1-7 and 37-41 of the present invention.

The specific claims of the present invention are discussed below.

A. **Claims 1-41 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by U.S. Patent No. 5,958,027 (*Gulick*) in view of U.S. Patent No. 6,021,129 (*Martin*).**

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all of the claims' limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom, is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to the alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990);

M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Appellants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Appellants respectfully assert that the Examiner did not meet the legal standards to reject the claims of the present invention under 35 U.S.C. § 103(a) because the prior art references (***Gulick*** and ***Martin***) do not teach or suggest all the claim limitations of the claims of the present invention. Additionally, the Examiner has not provided sufficient evidence or arguments that there is a suggestion that one skilled in the art would have been motivated to combine the references (***Gulick*** and ***Martin***). In fact, Appellants provide arguments that ***Gulick*** and ***Martin*** would not have been combined by one skilled in the art. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regards to claims 1-20 of the present invention.

Claims 1-19 stand rejected as unpatentable under 35 U.S.C. § 103(a) by U.S. Patent No. 5,958,027 (***Gulick***) in view of U.S. Patent No. 6,021,129 (***Martin***). Appellants respectfully assert that the Examiner erred in maintaining this rejection.

Group I Claims (Claims 1, 3, 4, and 7) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Gulick* in view of *Martin*.

Claim 1 of the present invention calls for an adaptive frame tracking unit that is capable of automatically adjusting a data rate of a data packet by determining whether there exists at least one data frame error. These features are not disclosed, taught, or made obvious by ***Gulick***, ***Martin***, or their combination. ***Martin*** clearly does not disclose automatically adjusting a data rate based upon a data frame error. In addition, ***Gulick***, which the Examiner uses to make up for the deficit of ***Martin***, also does not disclose adjusting a data rate based upon a data frame error. ***Gulick*** discloses monitoring a clock rate based upon the level of a buffer. Simply performing this monitoring does not equate to automatically adjusting a data rate of a data packet based upon a data frame error, as called for by claims of the present invention. The Examiner does not provide sufficient arguments or evidence to support a contention to the contrary.

In the Final Office Action dated January 31, 2005, the Examiner stated that ***Gulick*** teaches a USB host monitoring a clock rate and adjusting the clock rate based upon the level of the buffer and cited at column 7, line 35. (*See* page 3 of the Final Office Action dated January 31, 2005). However, this disclosure does not make obvious the concept of automatically adjusting a data rate of a data packet by determining if there exists at least one data frame error. Simply monitoring a clock rate based upon the level of a buffer does not equate to automatically adjusting a data rate of a data packet based upon a data frame error. The Examiner does not provide sufficient arguments or evidence to support a contention to the contrary.

In the Final Office Action dated January 31, 2005, the Examiner also stated that ***Martin*** does not teach a frame tracking unit capable of automatically adjusting the data rate based upon a data frame error, as called for by claim 1 of the present invention. The Examiner, however, erroneously argued that ***Gulick*** and ***Martin,*** in combination, disclose the elements of claim 1 of the present invention. The Examiner stated that ***Gulick*** does not disclose automatically adjusting the clock rate of a transmission rate. Appellants respectfully assert that since ***Gulick*** does not disclose adjusting a clock rate based upon a transmission rate, and ***Martin*** does not disclose frame tracking and adjusting a data rate based upon a data frame error, the combination of ***Gulick*** and ***Martin*** could not possibly disclose or make obvious automatically adjusting the data rate based upon a data frame error, as called for by claim 1 of the present invention.

Claim 1 of the present invention calls for an adaptive frame tracking unit that is capable of automatically adjusting a data rate of a data packet by determining whether there exists at least one data frame error. As conceded by the Examiner, ***Martin*** clearly does not disclose automatically adjusting a data rate based upon a data frame error. In addition, ***Gulick***, which the Examiner uses to make up for the deficit of ***Martin***, also does not disclose adjusting a data rate based upon a data frame error. In fact, the only mention of error in ***Gulick*** relates to a statement in the Background Section that indicates that constant data rate through a pipe is provided and in the case of delivery failure due to error, there is no attempt to retry to deliver the data in relation to a universal serial bus. *See* column 2, lines 52-55. Nowhere does ***Gulick*** disclose adjusting a data rate based upon a data frame error. The mere disclosure in ***Gulick*** disclosing that a mechanism is provided to adjust the clock rate of a data producer to match the data clock rate of a USB host does not read upon elements of claims of the present invention. *See* column 7, lines 35-37. ***Gulick*** merely discloses that the clock rate of the data producer is adjusted and it is not

practical to adjust the data rate of a USB host. *See* column 7, lines 37-39. This disclosure does not make obvious automatically adjusting a data rate of a data packet based upon a data frame error. The Examiner used improper hindsight reasoning to assert that ***Gulick*** provides adequate disclosure (in combination with ***Martin***) to make obvious all of the elements of claim 1 of the present invention.

Martin merely discloses modifying a scheduled time parameter associated with rescheduling of another cell from the same channel to compensate for transmission error. *See* column 14, lines 62-65. ***Martin*** clearly does not disclose adjusting of a data rate based upon a data frame error. As conceded by the Examiner in the Final Office Action dated January 31, 2005, ***Martin*** merely discloses a rate control module that may modify the rate of cell transmission, based upon a transmission rate associated with a particular group of ATM cells, or modify the rate to compensate for delays incurred during previous transmissions. *See*, col. 8, lines 25-38. ***Martin*** merely modifies the rate to compensate for delays that occurred in a previous transmission. *Id.* The Examiner erroneously equates this disclosure to the concept of automatically adjusting a data rate by determining whether a data frame error exists, as called for by claim 1 of the present invention. ***Martin*** simply does not check for a data frame error, and neither does ***Gulick***. The mere disclosure of the transmission manager 152 in ***Martin,*** in cooperation with the controller 40, to schedule and control the rate of transmission of signals received from a universal serial bus, simply does not anticipate or make obvious the adjusting of the data rate based upon determining whether a data frame error exists and then correcting the data frame error, as called for by claim 1 of the present invention.

The Examiner cited various passages of ***Martin*** that indicate that the transmission link 18 in ***Martin*** formats information to facilitate transmission of a universal serial bus (USB) and data

blocks comprising a plurality of ATM cells payloads in determining appropriate virtual channels to facilitate their transmission. The Examiner asserted that this disclosure equates to the adaptive frame tracking called for by claim 1 of the present invention. However, Appellants respectfully assert that ***Martin*** simply does not disclose frame tracking, much less the adaptive frame tracking called for by claims of the present invention. The ATM payloads and the data blocks comprising the ATM cell payloads is received by determining appropriate virtual channel to facilitate their transmission. In other words, virtual channels are selected to receive data. This does not make obvious or anticipate the adaptive frame tracking called for by claim 1 of the present invention. Various elements of claim 1 of the present invention are not disclosed, taught, or suggested by ***Martin***, ***Gulick,*** or their combination, contrary to the Examiner's contentions in the Final Office Action dated January 31, 2005. Therefore, claim 1 is allowable for at least these reasons.

The Examiner erroneously uses improper hindsight reasoning to pick-and-choose various portions of ***Martin*** and ***Gulick*** in an attempt to make obvious all of the elements of claim 1. For example, the Examiner concedes that ***Martin*** does not teach adaptive frame tracking and automatically adjusting a data rate based upon a frame error. The Examiner also concedes that ***Gulick*** does not specifically disclose teaching automatically adjusting the clock rate based upon a transmission rate. The Examiner then refers back to ***Martin*** to cite a controller that provides functionality to modify the transmission rate based upon a transmission delay of a previous transmission. However, even with the pick-and-choose approach utilized by the Examiner, the element of adaptive frame tracking for automatically adjusting a data rate based upon a frame error, as called for by claim 1 of the present invention, is not made obvious by the cited prior art. Therefore, the back and forth references between various portions of ***Martin*** and ***Gulick*** still do

not make obvious the automatic adjustment of data rate based upon a data frame error. Therefore, claim 1 is allowable or at least these reasons.

Additionally, the Examiner's combining of various pieces of ***Martin*** and ***Gulick*** is based upon improper hindsight reasoning. Simply because ***Gulick*** discloses a universal serial bus and an isochronous bus monitoring the data level of a buffer within the USB host does not, in combination with ***Martin,*** disclose, teach, or make obvious all of the elements of claim 1 of the present invention. Therefore, contrary to Examiner's arguments, those skilled in the art would not combine ***Gulick*** and ***Martin*** to make obvious all of the elements of claim 1 of the present invention. The Examiner has not provided evidence to the contrary.

As indicated by the Examiner in the Final Office Action dated January 31, 2005, it is clear that neither ***Gulick*** nor ***Martin***, by themselves could possibly disclose, suggest, or make obvious all of the elements of claim 1 of the present invention. The Examiner uses ***Martin*** to disclose the element of the automatic adjusting of a data rate based upon the adjustment of the transmission rate. However, other elements of claims of the present invention, such as a frame tracking unit capable of automatically adjusting a data rate based upon a data frame error, are not taught, disclosed, or made obvious by ***Martin***.

Furthermore, Appellants respectfully assert that ***Martin*** does not teach frame tracking, much less adaptive frame tracking, which is called for by claim 1 of the present invention. ***Martin*** merely mentions the term "frame" in the context of avoiding losing accuracy due to large frame rates of a USB communication. However, ***Martin*** does not disclose an adaptive frame tracking, as called for by claim 1 of the present invention. Additionally, even if ***Gulick*** and ***Martin*** were to be combined, all of the elements of claim 1 would not be taught, disclosed,

suggested, or made obvious. Additionally, claims 3, 4, and 7 also include the limitations of claim 1 by virtue of their dependencies to claim 1, therefore, are also allowable for at least the reasons cited above. The combination of ***Gulick*** and ***Martin*** does not provide for the adaptive frame tracking called for by the claims of the present invention. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regards to claims 1, 3, 4, and 7 of the present invention. Accordingly, the Examiner's rejections of claims 1, 3, 4, and 7 should be reversed and claims 1, 3, 4, and 7 should be allowed.

Independent claim 1 is allowable for at least the reasons cited above. Additionally, dependent claims 2-36 which depend from independent claim 1 are also allowable for at least the reasons cited above.

Group II Claims (Claims 2, 5, and 6) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Gulick* in view of *Martin*.

As described above, claim 1 of the present invention, from which claims 2, 5, and 6 depend, is not anticipated or made obvious by ***Gulick, Martin***, or their combination. For example, ***Gulick, Martin***, or their combination do not make obvious an adaptive frame tracking unit that is capable of automatically adjusting a data rate of a data packet by determining whether there exists at least one data frame error. These features are not disclosed, taught, or made obvious by ***Gulick***, ***Martin***, or their combination. As described above, ***Martin*** does not disclose automatically adjusting a data rate based upon a data frame error, as called for by claims 2, 5, and 6 of the present invention. ***Gulick***, which the Examiner uses to make up for the deficit of ***Martin***, also does not disclose adjusting a data rate based upon a data frame error. ***Gulick*** discloses monitoring a clock rate based upon the level of a buffer. This does not equate to

automatically adjusting a data rate of a data packet based upon a data frame error, as called for by claim 1 of the present invention.

Additionally, claims 2, 5, and 6 call for applying the adaptive frame tracking unit to data from a source relating to a universal serial bus (USB). For example, claims 5 and 6 call for receiving data from a USB host. ***Martin*** merely discloses a transmission manager 152 in cooperation with the controller 40 to schedule and control the rate of transmission of signals received from a USB. However, ***Martin*** simply does not anticipate or make obvious adjusting of the USB data rate based upon determining whether a data frame error exists and then correcting the data frame error, as called for by claims 2, 5, and 6. ***Gulick*** does not make up for this deficit. ***Gulick***, in the Background Section, mentions that constant data rate through a pipe is provided and in the case of delivery failure due to error, there is no attempt to retry to deliver the data in relation to a USB. *See* column 2, lines 52-55. However, ***Gulick*** does not disclose adjusting a data rate based upon a data frame error relating to data from a USB host. Accordingly, the disclosure of ***Gulick***, ***Martin***, or their combination, do not anticipate or make obvious all of the elements of claims 2, 5 and 6. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regards to claims 2, 5, and 6 of the present invention. Accordingly, the Examiner's rejections of claims 2, 5, and 6 should be reversed and claims 2, 5, and 6 should be allowed.

Group III Claims (Claims 8-36) Are Allowable.

The Examiner did not reject claims 8-36. The Examiner objected to claims 8-36. Appellants respectfully assert that claims 8-36 are not anticipated or make obvious by ***Gulick***, ***Martin***, or their combination, for at least the reasons cited above (*See* arguments under Group I

Claims section above). Appellants believe that the Examiner objected to claims 8-36 simply because they depend from rejected claims. However, Appellants believe that the Examiner agrees that claims 8-36 contain allowable subject matter, and that claims 8-36 would have been allowed had they not been depended from rejected claims. In light of the arguments provided herein Appellants respectfully assert that the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regards to claim 1, from which claims 8-36 directly or indirectly depend. Accordingly, the Examiner's objections with regards to claims 8-36 should be reversed and claims 8-36 should be allowed.

Group IV Claims (Claims 37-41) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Gulick* in view of *Martin*.

Appellants respectfully assert that claims 37-41 are not anticipated or made obvious by ***Gulick, Martin***, or their combination. Claim 37 calls for a method for performing adaptive frame tracking. The method includes monitoring a data packet from a data stream and supporting transmit data buffering of said data packet. The method also includes determining whether at least one data packet is missing from a received data stream and establishing a start of frame rate control for said data packet for said missing data packet. The method also calls for performing an auto rate control of the data packet. Further, claim 41 calls for an apparatus for performing an adaptive frame tracking that includes means for monitoring a data packet from a data stream and supporting transmit data buffering of said data packet. Claim 41 also calls for means for determining whether at least one data packet is missing from a received data stream and means for establishing a start of frame rate control for said data packet for said missing data packet. Claim 41 also calls for means for performing an auto rate control of the data packet.

These are elements that are not anticipated or made obvious by ***Gulick, Martin***, or their combination.

Neither ***Gulick*** nor ***Martin*** disclose performing an auto rate control of the data packet, as called for by claims 37 and/or 41 of the present invention. Further, neither ***Gulick*** nor ***Martin*** disclose or make obvious determining if a data packet is missing and establishing a start of frame rate control for the missing data packet, as called for by claims 37 and 41 of the present invention. ***Martin*** merely mentions the term "frame" in the context of avoiding losing accuracy due to large frame rates of a USB communication. However, ***Martin*** does not disclose an adaptive frame tracking or establishing a start of frame rate control for the missing data packet, as called for by claim 37 and 41. ***Martin*** clearly does not disclose adjusting of a data rate based upon a data frame error. ***Martin*** merely discloses a rate control module that may modify the rate of cell transmission, based upon a transmission rate associated with a particular group of ATM cells, or modify the rate to compensate for delays incurred during previous transmissions. *See*, col. 8, lines 25-38. ***Martin*** merely modifies the rate to compensate for delays that occurred in a previous transmission. *Id.* However, this disclosure does not make obvious determining if a data packet is missing and establishing a start of frame rate control for the missing data packet, or performing an auto rate control of the data packet. ***Gulick*** discloses monitoring a clock rate based upon the level of a buffer. However, simply performing this monitoring does not equate to determining if a data packet is missing and establishing a start of frame rate control for a missing data packet, or performing an auto rate control of the data packet. In other words, the combination of ***Gulick*** and ***Martin*** does not disclose or make obvious establishing a start of frame rate control for a missing data packet, or performing an auto rate control of the data packet, as called for by claims 37 and 41 of the present invention.

Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regarding to claims 37 and 41 of the present invention. Independent claims 37 and 41 are allowable for at least the reasons cited above. Additionally, dependent claims 38-40, which depend from independent claim 37 are also allowable for at least the reasons cited above. Accordingly, the Examiner's rejections of claims 37-41 should be reversed and claims 37-41 should be allowed.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 1-41) pending in the present application over the prior art of record. **The undersigned attorney may be contacted at (713) 934-4069** with respect to any questions, comments, or suggestions relating to this appeal.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
CUSTOMER NO. 23720

Date: July 5, 2005

By: _____

Jaison C. John, Reg. No. 50,737
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-7000
(713) 934-7011 (facsimile)
ATTORNEY FOR APPLICANT(S)

APPENDIX A

1. (Original) An apparatus for performing adaptive frame tracking, comprising an adaptive frame tracking unit capable of receiving and sending at least one data packet and automatically adjusting a data rate of said data packet by determining if there exists at least one data frame error and correcting for said data frame error in response to a determination that there exists at least one said data frame error.

2. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit receives and sends at least one universal serial bus data packet.

3. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit is capable of receiving a frame of data from a computer peripheral device and perform adaptive frame tracking upon said frame of data and transmitting said frame of data.

4. (Previously presented) The apparatus of claim 3, wherein said computer peripheral device is one of a computer modem, a scanner, a multimedia system, a computer mouse, and an external data read/write device.

5. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit is capable of receiving a frame of data from a universal serial bus host and performing adaptive frame tracking upon said frame of data and transmitting said frame of data.

6. (Previously presented) The apparatus of claim 3, wherein said universal serial bus host is a computer system.

7. (Original) The apparatus of claim 1, wherein said data frame error further comprises a missing start of scan data pattern.

8. (Original) The apparatus of claim 1, wherein said adaptive frame tracking unit comprises:

a start of frame synthesizer circuit for monitoring data streams and determining whether there exists a start of frame data packet and performing a start of frame synthesis in response to a determination that a start of scan does not exist;

a frame position monitor circuit coupled with said start of frame synthesizer for generating a frame position monitor sample clock and a latched frame count signal;

an auto data rate control circuit, said auto data rate control circuit being coupled with said start of frame synthesizer circuit and said frame position monitor circuit, for generating a data packet size signal to determine a number of bytes to be received in said data frame; and

a frame number monitor circuit, said frame number monitor circuit being coupled with each of said start of frame synthesizer circuit, said frame position monitor circuit, and said auto data rate control circuit, for determining a present data frame number value and generating a time stamp match signal for determining whether a

frame number corresponding to a data frame that has a missing start of frame data packet.

9. (Original) The apparatus of claim 8, wherein said adaptive frame tracking unit is capable of performing adaptive synchronization.

10. (Original) The apparatus of claim 8, wherein said start of frame data packet comprises of a sync data field, a packet identification data field, a frame number field, a CRC5 bit, and an end of packet data field.

11. (Original) The apparatus of claim 8, wherein said start of frame synthesizer circuit comprises:

a frame counter for generating at least one data frame signal;

an error counter electronically coupled with said frame counter for generating a start of frame status signal; and

a set of digital logic electronically coupled with said frame counter and said error counter for generating at least one said data frame signal and said frame status signal.

12. (Original) The apparatus of claim 11, wherein said start of frame synthesizer circuit is capable of tracking a number of bits in a frame of data.

13. (Original) The apparatus of claim 11, wherein said start of frame synthesizer circuit is capable of detecting a missing start of frame data pattern.

14. (Original) The apparatus of claim 11, wherein said start of frame synthesizer circuit is capable of performing a start of frame synthesis.

15. (Original) The apparatus of claim 11, wherein said data frame signal further comprises of a frame count signal.

16. (Original) The apparatus of claim 11, wherein said frame status signal further comprises of a synthesized start of frame signal.

17. (Original) The apparatus of claim 11, wherein said frame status signal further comprises of a missed start of frame signal.

18. (Previously Presented) The apparatus of claim 8, wherein said frame position monitor circuit further comprises:

a dividing counter for dividing at least one clock signal;

a frame count register logically coupled with said clock signal for latching a frame count signal; and

a set of digital logic electronically coupled with said dividing counter and said frame count register for generating said clock signal and latching said frame count signal.

19. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of performing a start of frame mastership.

20. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of generating a frame position monitor sample clock.

21. (Original) The apparatus of claim 20, wherein said frame position monitor circuit is capable of dividing said frame position monitor sample clock by a plurality of values.

22. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of generating a frame position updated signal.

23. (Original) The apparatus of claim 18, wherein said frame position monitor circuit is capable of generating a latch frame count signal.

24. (Original) The apparatus of claim 8, wherein said auto rate control circuit further comprises:

an auto rate counter for generating a data frame count value;

an auto rate register for latching said data frame count value generated by said auto rate counter;

an auto rate controller for controlling said auto rate counter and said auto rate register; and

a left-shifter multiplier for multiplying a latched data frame count value by one of a plurality of values.

25. (Original) The apparatus of claim 24, wherein said auto rate control circuit is capable of controlling a data rate of an data endpoint.

26. (Original) The apparatus of claim 25, wherein said data endpoint is an isochronous data endpoint.

27. (Original) The apparatus of claim 24, wherein said auto rate control circuit is capable of generating a data packet size signal.

28. (Original) The apparatus of claim 27, wherein said data packet size signal is an isochronous packet size signal.

29. (Original) The apparatus of claim 28, wherein said auto rate control circuit is capable of sending said isochronous packet size signal to a data endpoint.

30. (Original) The apparatus of claim 24, wherein said auto rate counter is incremented by said auto rate controller using a frame position sample monitor clock.

31. (Original) The apparatus of claim 24, wherein said auto rate controller is capable of clearing and re-enabling said auto rate counter.

32. (Original) The apparatus of claim 8, wherein said frame number monitor circuit further comprises:

a frame number monitor counter for latching a frame number signal and generating a latched frame number monitor signal;

a time stamp match register for generating a time stamp match signal using said latched frame number monitor signal; and

a set of digital logic electronically coupled with said frame number monitor counter and said time stamp match register for latching said frame number signal and generating a time stamp match signal.

33. (Original) The apparatus of claim 32, wherein said frame number monitor counter increments said latched frame number signal in response to an assertion of a missed start of frequency signal.

34. (Original) The apparatus of claim 32, wherein said frame number monitor circuit generates said time stamp match signal in response to a determination that said latched frame number signal is one of equal to and greater than a time stamp match value signal.

35. (Original) The apparatus of claim 32, wherein said latched frame number monitor signal contains a universal serial bus frame number value.

36. (Original) The apparatus of claim 32, wherein said time stamp match register can be loaded with data using a software control.

37. (Previously Presented) A method for performing adaptive frame tracking, comprising:

monitoring at least one data packet from a data stream;

supporting transmit data buffering of said data packet;

determining whether at least one data packet is missing from a received data stream;

establishing a start of frame rate control for said data packet for said missing data packet; and

supporting an auto rate control of said data packet.

38. (Original) The method of claim 37, wherein receiving and sending at least one data packet from a data stream further comprises receiving universal serial bus isochronous data packets.

39. (Original) The method of claim 37, wherein determining whether at least one data packet is missing from a received data stream further comprises performing start of frame error checking.

40. (Original) The method of claim 37, wherein supporting an auto rate control of said data packet further comprises automatically adjusting a data rate of said data packets to match a data rate of a universal serial bus communication system.

41. (Previously Presented) An apparatus for performing adaptive frame tracking, comprising:

means for receiving and sending at least one data packet from a data stream;

means for supporting transmit data buffering of said data packet;

means for determining whether at least one data packet is missing from a received data stream;

means establishing a start of frame rate control for said data packet for said missing data packet; and

means for supporting an auto rate control of said data packet.